

Toward Photonic Integrated Circuits

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Integration

Introduction: - Criteria
- Optical Logic Gate

Levels: - Small/Medium Scale
Cascadability
- Medium Scale
- Large Scale
Heat



Integration Criteria

Low Loss:

- Minimize reflections:
 - match index of refraction
 - match mode profile
- Minimize material absorption
- Minimize radiation
 - large index contrast between waveguide and surroundings

Polarization Insensitivity

Optical Component Interaction

- Active devices with passive waveguides

Wide Operating Space

- Wavelength
- Temperature

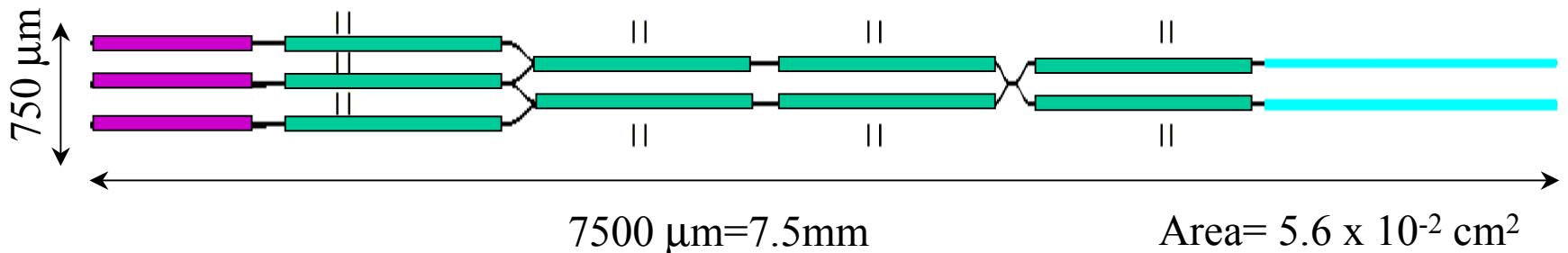
Photonic/Electronic Interaction

- Connections
- Circuitry

Package Mechanically Stable Manufacturable

More Robust Logic Gate

Structure Layout:



Individual Components:

- 9 **SOAs** each 1 mm long
 - 5 for amplification, 4 for phase shifts
- 10 to 18 contacts each $50 \mu\text{m} \times 50 \mu\text{m}$
- 3 **Isolators** each 1mm long
- 2 **Bragg filters** each 1.5 mm long



Logic Gate: The Numbers

Mach-Zehnder Interferometer Semiconductor Optical Amplifier Based Logic

Per Robust Logic Gate

| Component | Purpose | Number Needed | Loss | Electrical Power | Dimensions | Estimated Total |
|----------------------|-------------|---------------|--|---------------------------|---------------------------------------|---|
| SOA | Gain | 0 to 5 | Provides Gain | 0.2W (~1V at ~200mA) each | 0.5 μm(w) x 1 μm (h) x 1mm (l) each | 0 to 1 W 0 to 25 x 10 ⁻⁶ cm ² 0 to 3 x 10 ⁻⁴ cm ² |
| SOA | Phase shift | 4 | Variable | 0.1W (~1V at ~100mA) | 0.5 μm(w) x 1 μm (h) x 1mm (l) | 0.4 W 20 x 10 ⁻⁶ cm ² 2 x 10 ⁻⁴ cm ² |
| Y-Coupler / Splitter | | 5 | (see bends) | Passive | ~200μm (w) x ~100s μm (l) | ~10 x 10 ⁻⁴ cm ² |
| Bends | | ~20 | Smaller the radius, the higher the loss | Passive | Radius ?100um | ~20 x 10 ⁻⁴ cm ² |
| Waveguides | | ~1-2 mm | ~0dB to 5 dB/cm | Passive | 0.5 μm(w) x 0.2 μm (h) | |
| Waveguide Crossing | | 1 | | Passive | 0.5 μm(w) x 0.2 μm (h) | |
| Filters | | 0 to 2 | ~ 0dB on resonance ~ -25 dB off resonance | Passive | 0.5 μm(w) x 0.2 μm (h) x 4mm (l) each | 0 to 40 x 10 ⁻⁶ cm ² |
| Isolators | | 0 to 3 | 17 dB extinction ratio | Passive | 230 μm (l) | |

Contacts=50 μm x 50 μm



Integration Assumptions

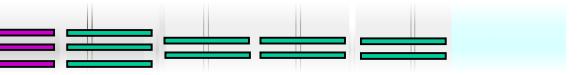
- No reduction in complexity due to different architectures
- No reduction in size due to high index contrast
- Simple *linear extrapolation* of the optical logic gate with isolators, filters, pre and post amplifiers;
- No specific design implied
- In a “real” design, different optical components may be required



Small/Medium Scale Integration

Number of Gates: ~10

Number of active components: ~(40 to 90)



Applications: ReAmplification, ReShaping, ReTiming
OTDM Transceiver

Approaches: Monolithic Integration
Hybrid Integration

Estimated Power and Die Sizes:

Monolithic: ~(4 to 14) Watts in a die ~(0.2 to 0.5) cm² (~0.8 cm x ~0.6 cm)

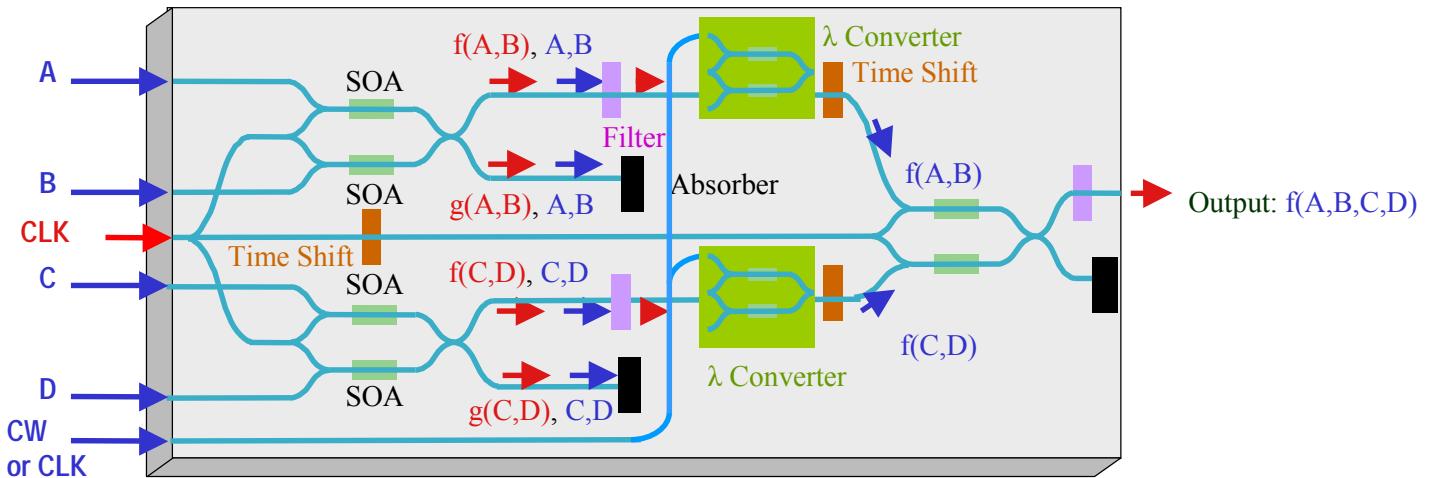
Hybrid: ~(4 to 14) Watts in a module ~10 cm x ~6 cm

Integration Issues: Monolithic: External electronics may be possible ~200 pins,
optical path length matching

Hybrid Approach: alignment of multiple SOA arrays,
yield, reliability, large dies/modules

Alignment of multiple fibers

Cascadability



Optical Issues:

- 1) Significant amount of space is used for waveguide bends
- 2) Multiple wavelengths are utilized within the die
- 3) Multiple wavelength clocks/control signals required for cascading optical logic elements.
- 4) Reflections must be taken into account
- 5) Optical path lengths must be equal

Design Issues:

- 6) Optical design library required
- 7) “Pulse” logic design rules are required
- 8) Design methodologies for connectivity required.
- 9) Design methodologies for testability required
- 10) Robust simulation software required

Practical Issues

- 11) A location for the electronics is required
- 12) The MZ-SOA combinations require initialization.
- 13) Photonic integrated circuits must be manufacturable.



Medium Scale Integration

Number of Gates: ~100

Number of active components: ~400 to 900

Applications: 16 x 16 Packet Switching

Stronger Forward Error Correction

Weak Encryption

Estimated Power and Die Sizes:

Optical: ~(40 to 140) Watts in a die ~(2 to 5) cm²

Electronic: Assume die size 0.04 cm x 0.04 cm/SOA => 1.28 cm²

Integration Issues: Integrated bias and control electronics

Requires both space and electrical power

Requires both digital and analog electronics

Requires integrated switches, photodetectors, sources, optical clocks,
variable time delays (optical path length matching)

Optical logic gate testability

Optical logic gate library/Design rules

Alignment of multiple fibers



Heat

Optical Integration Level

| | Power (W) | cm ² | W/cm ² |
|----------------------------|-----------|-----------------|-------------------|
| Small* | ~3.6 | 1 | ~3.6 |
| Small/Medium* | ~12 | 1 | ~12 |
| Medium (100) | ~150 | 5 | ~30 |
| Large (10000) ⁺ | ~9000 | ~200 | ~45 |

* Assumes 1 cm² monolithic dies

⁺ Assumes a 2x increase in density

Si Road Map (MPUs)

| Year | W | cm ² | W/cm ² |
|-------|-----|-----------------|-------------------|
| 2003: | 150 | 3.64 | 41 |
| 2005: | 170 | 4.54 | 37 |
| 2007: | 190 | 5.68 | 33 |
| 2010: | 218 | 5.63 | 38 |
| 2013: | 251 | 3.73 | 67 |

High power lasers typically have a wall plug efficiency of 50%

=> ~ 50% of the electrical power converted to heat

TE Cooler Performance*

Size: 0.8 x 0.8 cm to 5.5 x 5.5 cm

Cooling capacity: 1 W (1.9A, 0.9V) to 186 W (78A, 3.9V) ($\sim 0.6 \text{ W}_{\text{thermal}}/\text{W}_{\text{electrical}}$)

$\Delta T_{\max} = 70\text{K}$

* Kryo Therm Products

End of Presentation